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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/971,991	10/04/2001	Kyu-Nam Lim	AB-984-1C US	5338

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EXAMINER
NGUYEN, LINH M

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/971,991	LIM, KYU-NAM	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-10 and 12-24* is/are rejected.

7)☒ Claim(s) *7 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/574,306* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-24 are presented in the instant application according to the Applicants' RCE and amendment filing on 06/11/2003.

Title

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: " AN INPUT BUFFER CIRCUIT SIMULTANEOUSLY SUPPORTS A LOW VOLTAGE INTERFACE AND A GENERAL LOW VOLTAGE TRANSISTOR LOGIC (LVVTL) INTERFACE ".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-10, and 12-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Pryor (U.S. Patent No. 3,991,380).

With respect to claims 1, 4, 8, and 12, Figure 2 of Pryor shows an input buffer circuit comprising a) a first inverting switch [10] connected to a first input voltage [11] and outputting a self bias signal [12]; b) a second inverting switch [20] connected to a second input voltage [21] and outputting an output signal [22]; c) a gain control unit [50, P8, N8] having a dual feedback loop *(1st feedback loop: 12, P-3,P-4, NODE A, 53,P-5, 51, 12; 2nd feedback loop: 12, N-3, N-4, NODE B, 54, N-5, 51, 12)* for gain control responsive to the self bias signal [12] and the output

signal; d) a current controlling circuit [30,40] that supplies current to the first inverting switch, the second inverting switch and the gain control unit, sinks current from the first inverting switch, the second inverting switch and the gain control unit, and responds to the self bias signal; and e) a swing width control circuit connected to a feedback signal that is inverted by the output signal.

With respect to claims 2, 5, and 9, Fig. 2 of Pryor shows that the gain control unit comprises a) a first PMOS transistor [P5] having a source connected to a first node, a drain connected to the self bias signal, and a gate connected to the output signal; b) a first NMOS transistor [N5] having a source connected to a second node, a drain connected to the self bias signal, and a gate connected to the output signal; c) a second PMOS transistor [P6] having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and d) a second NMOS transistor [N6]having a source connected to the second node, a drain connected to the output signal, and a gate connected to the self bias signal.

With respect to claims 3, 6, and 10, Fig. 2 of Pryor shows that the gain control unit further comprises: a) a third PMOS transistor [P8] having a source connected to the first node, a gate and a drain connected to the self bias signal; and b) a third NMOS transistor [N8] having a source connected to the second node, a gate and a drain connected to the self bias signal.

With respect to claims 13, 16, 19, and 22, Pryor discloses, in Fig. 2, that the dual feedback loop includes a first feedback loop including at least one node and at least one PMOS transistor and a second feedback loop including at least one node and at least one NMOS transistor.

With respect to claims 14, 17, 20 and 23, Pryor discloses, in Fig. 2, that the first feedback loop, the self bias signal is supplied to a first node, a gate of a first PMOS transistor, a gate of a second PMOS transistor, a second rode, a source of a third PMOS transistor and back to the first node to complete the first feedback loop.

With respect to claims 15, 18, 21 and 24, Pryor discloses, in Fig. 2, that the second feedback loop, the self bias signal is supplied to a first node, a gate of a first NMOS transistor, a gate of a second NMOS transistor, a source of a third NMOS transistor and back to the first node to complete the second feedback loop.

Allowable Subject Matter

4. Claims 7 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Prior art of record does not show or fairly suggest (1) the current controlling circuit being comprised of: a) a third PMOS transistor having a source connected to the first node, a drain connected to the gain control unit to supply current and a gate connected to the self bias signal; and b) a third NMOS transistor having a source connected to the second node, a drain connected to the gain control unit to sink current and a gate connected to self bias signal, as called for in claim 7, and (2) the width control circuit being comprised of : a) an NMOS transistor having a source connected to the gain control unit, a drain connected to the gain control unit and a gate connected to the feedback signal; and b) a PMOS transistor having a source connected to the output signal, a drain connected to the gain control unit and a gate connected to the feedback signal, as called for in claim 11.

Remarks and Conclusion

6. Applicant's arguments filed 06/11/2003 have been fully considered but they are not persuasive.

With respect to amended claims 1, 4, 8 and 12, at page 12, second paragraph, Applicant stated that *" a dual feedback loop as recited in independent claims 1,4, 8 and 12 is not taught or suggested by Pryor "*. The Examiner disagrees since Pryor clearly discloses, in Fig. 2, a dual feedback loop with first feedback loop comprising elements 12, P-3, P-4, NODE A, 53,P-5, 51, 12; and second feedback loop with elements 12, N-3, N-4, NODE B, 54, N-5, 51, 12. Thus claims 1-6, 8-10, and 12 are still being rejected under 35 U.S.C. §102(b) as being anticipated by Pryor.

Inquiry

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and (703) 305-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Linh M. Nguyen
Examiner
Art Unit 2816

LMN
July 17, 2003